LM389
F4093
NEC 8246 K8005
D416C-2

National Semiconductor

LM1872 Radio Control Receiver/Decoder

General Description

The LM1872 is a complete RF receiver/decoder for radio control applications. The device is well suited for use at either 27 MHz, 49 MHz or 72 MHz in controlling various toys or hobby craft such as cars, boats, tanks, trucks, robots, planes, and trains. The crystal controlled superhet design offers both good sensitivity and selectivity. When operated in conjuction with the companion transmitter, LM1871, it provides four independent information channels. Two of these channels are analog pulse width modulated (PWM) types, while the other two are simple ON/OFF digital channels with 100 mA drive capability. Either channel type can be converted to the other form through simple external circuitry such that up to 4 analog or up to 4 digital channels could be created. Few external parts are required to complement the self-contained device which includes local oscillator, mixer, IF detector, AGC, sync output drivers, and all decoder logic on-chip.

Features

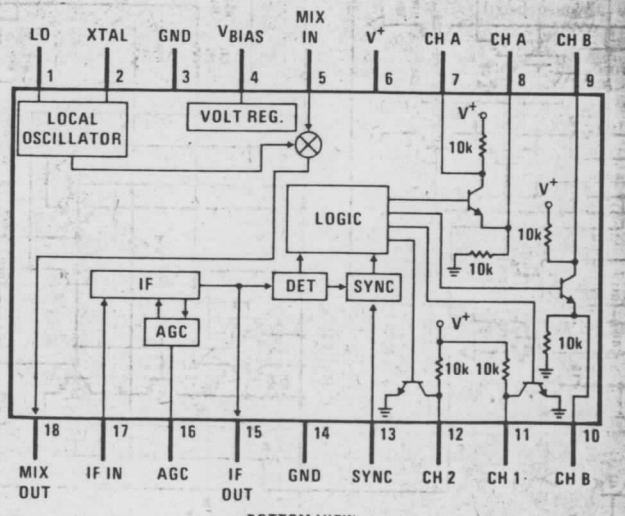
- Four independent information channels; two analog and two digital
- Completely self-contained
- Minimum of external parts
- Operation from 50 kilohertz to 72 MHz
- Highly selective and sensitive superhet design
- Operates from four 1.5V cells
- Excellent supply noise rejection
- 100 mA digital output drivers
- Crystal controlled
- Interfaces directly with standard hobby servos

Applications

- Toys and hobby craft
- Energy saving, remotely switched lighting systems
- Burglar alarms
- Industrial and consumer remote data links
- IR data links
- Remote slide projector control

Circuit Block and Connection Diagram

Dual-In-Line Package



BOTTOM VIEW

Order Number LM1872N

See NS Package N18A

Absolute Maximum Ratings

Supply Voltage	7V
Package Dissipation (Note 2)	1000 mW
Voltage @ Pin 7, 8, 9, 10, 11 or 12	V^+
Operating Temperature Range	−25 °C to +85 °C
Storage Temperature Range	−65 °C to +150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C

DC Electrical Characteristics

$V^+ = 6V$, $T_A = 25\,°C$, Test Circuit of *Figure 1*, $f_{LO} = 49.890$ MHz, $f_{IF} = 455$ kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	Functional for $V_{IN} = 100\ \mu V$	2.5	6	7	V
Supply Current	CH A & B Off		9	13	mA
	CH A & B On			27	mA
V_{BIAS}	@ Pin 4	1.85	2.1	2.35	V
Sync Timer Threshold	@ Pin 13, Going from Low to High Voltage	$V^+/2 - 0.4$	$V^+/2$	$V^+/2 + 0.3$	V
Digital Channels A and B					
Saturation Voltage	@ Pins 7 & 9, $R_L = 100\Omega$		0.4	0.7	V
Saturation Resistance	@ Pins 7 & 9		7		Ω
Source Current	@ Pins 8 & 10, $V_{Pin\ 8\ \&\ Pin\ 10} \leq 1V$	100			mA
Collector Pull-Up Resistance	Pin 7 & Pin 9 to V^+	5	10	20	kΩ
Emitter Pull-Down Resistance	Pin 8 & Pin 10 to GND	5	10	20	kΩ
Analog Channels 1 and 2					
Saturation Voltage	@ Pins 11 & 12, $R_L = 2$ kΩ		0.45	0.7	V
Saturation Resistance	@ Pins 11 & 12		160		Ω
Collector Pull-up Resistance	Pin 11 & Pin 12 to V^+	5	10	20	kΩ

AC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
RF Sensitivity	For "Solid" Decoded Outputs (Note 1)		22	39	μV
RF Sensitivity	Circuit of *Figure 5* @ 49 MHz with Antenna Simulation Network of *Figure 6*		12		μV
Voltage Gain	Pin 5 to Pin 15		58		dB
PSRR of RF Sensitivity	$3V \leq V^+ \leq 6V$		−1		%Δ/V
BW	3 dB Down @ Pin 15		3.2		kHz
Noise	Referred to Input, Pin 5, $V_{IN} = 0$		0.35		μVrms
	Referred to IF, Pin 15, $V_{IN} = 0$		0.28		mVrms
AGC Threshold	Onset of AGC Relative to RF Input, V_{IN}, @ Pin 5		88		μV
	Relative to IF Output @ Pin 15	$V^+ + 0.07$	$V^+ + 0.100$	$V^+ + 0.13$	V
Mixer Conversion Transconductance	From Pin 5 to Pin 18 @ 1 MHz	2.9	4.0	6.9	mmhos
	@ 27 MHz		3.7		mmhos
	@ 49 MHz		3.5		mmhos
Mixer Input Impedance	Pin 5 to Pin 4 @ 49 MHz (See Curves)		20 kΩ + 5 pF		

AC Electrical Characteristics (Continued)

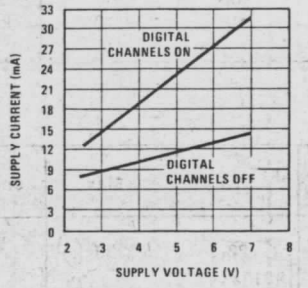
Parameter	Conditions	Min	Typ	Max	Units
Mixer Output Impedance	Pin 18 to GND		250		kΩ
IF Transconductance	Pin 17 to Pin 15 (AGC Off)@455 kHz	2.6	4.1	5.6	mmhos
IF Input Impedance	Pin 17 to GND		5500		Ω
IF Output Impedance	Pin 15 to GND (AGC Off) (AGC On)		800 2		kΩ MΩ
IF Carrier Level	@ Pin 15, V_{IN} = 100 μV (AGC On)		70		mVrms
Detector Threshold	Relative to RF Input, V_{IN}, @ Pin 5		20		μV
	Relative to IF Output @ Pin 15	V^+ + 0.015	V^+ + 0.025	V^+ + 0.040	V
Analog Pulse Width Accuracy	Ratio of Received Pulse Width @ Pins 11 & 12 to Transmitted Pulse Width @ Pin 5 for V_{IN} = 100 μV	0.95	1.0	1.05	ms/ms

Note 1: The criteria for the outputs to be considered "solid" are as follows:
DIGITAL: In order to check the decoding section, four RF frames are inputted in sequence with the proper codes to exercise all four possible logical output combinations at pins 7 and 9. For each frame the proper output logic state must exist.
ANALOG: Each analog pulse width (measured at pins 11 & 12) in any of the above four successive frames must not vary more than ±5% from the pulse widths obtained for V_{IN} = 100 μV.

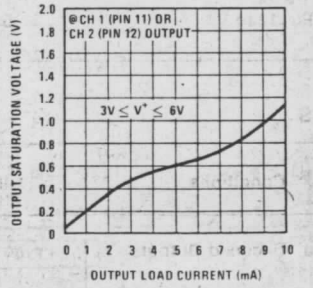
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 120°C/W, junction to ambient.

Typical Performance Characteristics

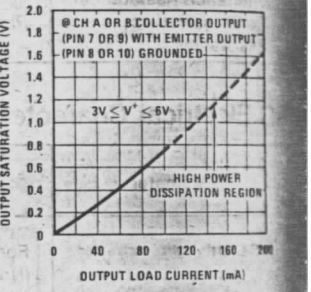
Supply Current vs Supply Voltage



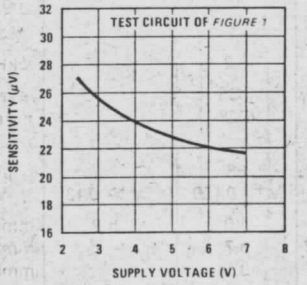
Analog Channel Output Voltage vs Load Current



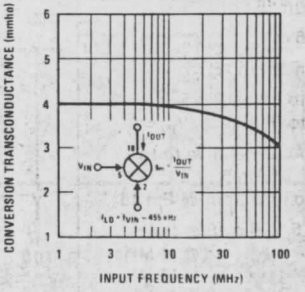
Digital Channel Collector Output Voltage vs Load Current


@ CH A OR B COLLECTOR OUTPUT (PIN 7 OR 9) WITH EMITTER OUTPUT (PIN 8 OR 10) GROUNDED
3V ≤ V⁺ ≤ 6V
HIGH POWER DISSIPATION REGION
OUTPUT SATURATION VOLTAGE (V)
OUTPUT LOAD CURRENT (mA)

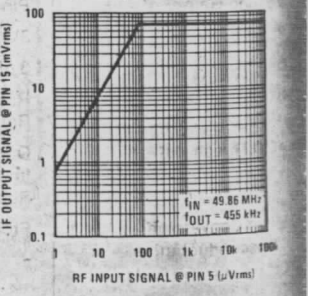
Sensitivity vs Supply Voltage



Mixer Transconductance (g_m) vs Input Frequency



IF Output Signal Level vs RF Input Signal Level



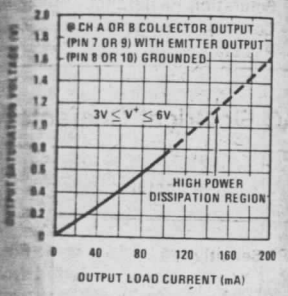
	Typ	Max	Units
	250		kΩ
	4.1	5.6	mmhos
	5500		Ω
	800		kΩ
	2		MΩ
	70		mVrms
	20		μV
	$V^+ + 0.025$	$V^+ + 0.040$	V
	1.0	1.05	ms/ms

codes to exercise all four possible logical out-

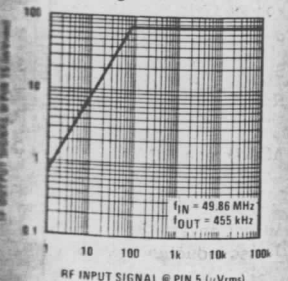
must not vary more than ±5% from the pulse

maximum junction temperature and a package

Digital Channel Collector Output Voltage vs Load Current

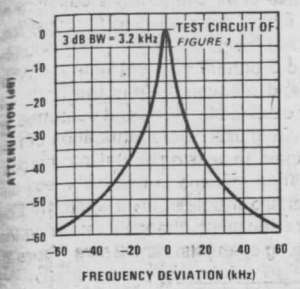

@ CH A OR B COLLECTOR OUTPUT
(PIN 7 OR 9) WITH EMITTER OUTPUT
(PIN 8 OR 10) GROUNDED
3V ≤ V+ ≤ 6V
HIGH POWER DISSIPATION REGION
OUTPUT LOAD CURRENT (mA)

IF Output Signal Level vs RF Input Signal Level

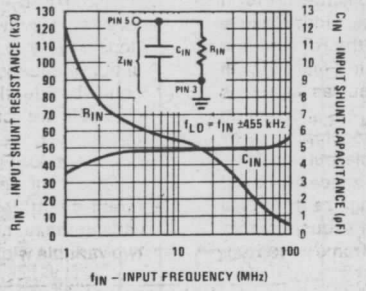


Typical Performance Characteristics (Continued)

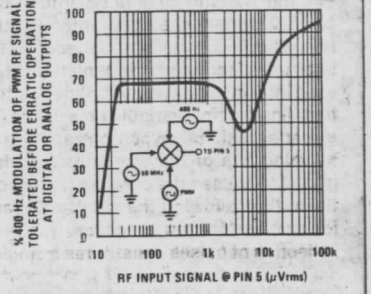
IF Bandpass Response



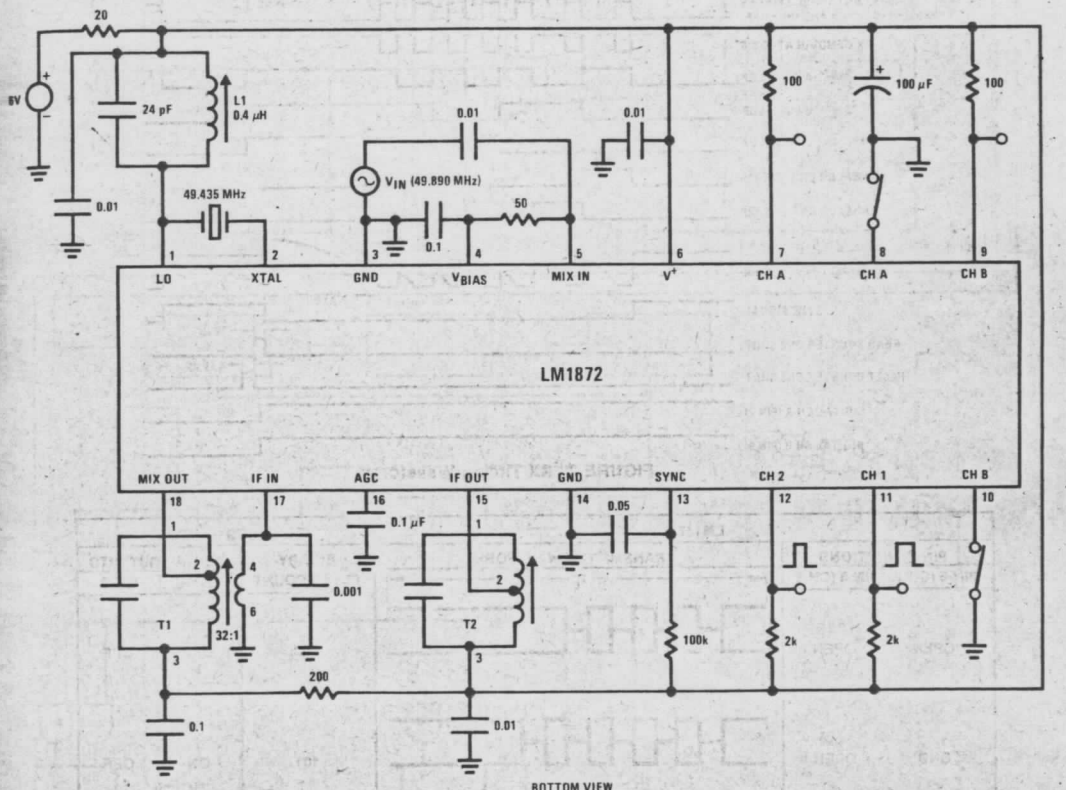
Equivalent Mixer Input Shunt Resistance and Capacitance vs Frequency



Receiver AM Rejection vs RF Input Level


% 400 Hz MODULATION OF PWM RF SIGNAL TOLERATED BEFORE ERRATIC OPERATION AT DIGITAL OR ANALOG OUTPUTS
400 Hz
10 PIN 5
30 MHz
PWM
RF INPUT SIGNAL @ PIN 5 (μVrms)

Test Circuit



L1 = Toko* 10k type (KEN-4028 DZ); 6T
T1 = Toko* 10 EZC type (RMC 202313 NO), Qu = 110
Pin 1-2, 131T; pin 2-3, 33T
Pin 1-3, 164T; pin 4-6, 5T

T2 = Toko* 10 EZC type (RMC 402503 NO), Qu = 110
Pin 1-2, 98T; pin 2-3, 66T
Pin 1-3, 164T; pin 4-6, 8T

* Toko America, Inc.
5520 West Touhy Ave.
Skokie, Ill. 60077
(312)677-3640 Tlx: 72-4372

FIGURE 1. Test Circuit

Circuit Description

The following discussion is best understood by referring to *Figures 2, 3, 4, and 5.*

SYSTEM ENCODING AND DECODING SCHEME

For the transfer of analog information, the LM1871/LM1872 system uses conventional pulse width modulation (PWM). In applying this technique, the RF carrier is interrupted for short fixed intervals (t_M in *Figure 2*) with each interval followed by variable width pulses (t_{CH}) so as to define multiple variable time spans ($t_M + t_{CH}$) occurring in serial fashion. Synchronization is accomplished by allowing one of the transmitted variable pulse widths (t_{SYNC}) to exceed the duration (t'_{SYNC}) of a receiver-based timer, thus allowing the receiver to recognize this pulse for synchronization purposes. Taken in sequence, this collection of pulses constitutes a single frame period (t_F).

The LM1871 transmitter is equipped to transmit up to six channels which the companion LM1872 receiver uses to derive 2 analog and 2 digital channels. The receiver decodes the demodulated RF waveform from the transmitter by negative edge triggering a cascade of three binary dividers called the A, B, and C toggle flip-flops *(Figure 4)*. By "examining" all three flip-flop outputs simultaneously, up to 6 unique channel time intervals could be identified and recovered. Only the first two channels are actually decoded however and outputted by the receiver, the rest being used for identification of two digital (ON/OFF) channels. In passing digital information, a pulse count modulation scheme is used whereby different quantities of channel pulses are transmitted by varying the number of fixed width channels following the two variable width analog channels 1 and 2 *(see Figure 3)*.

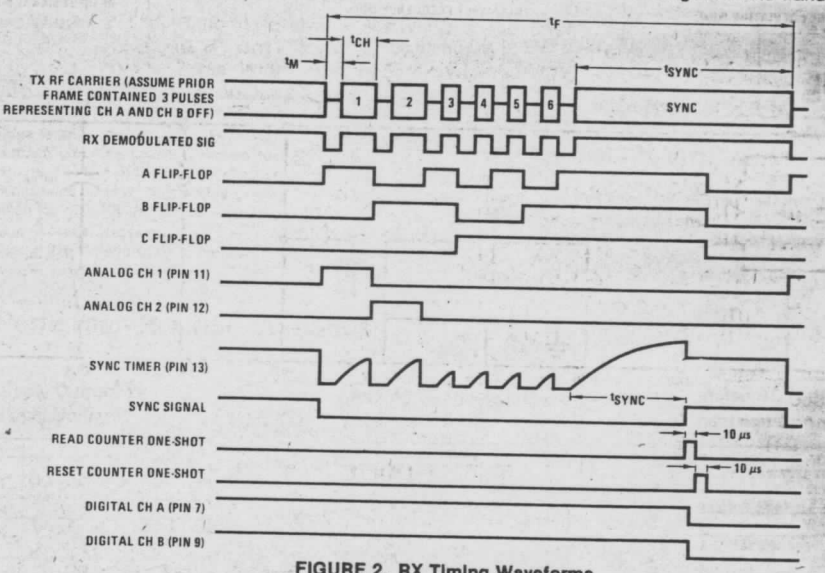


FIGURE 2. RX Timing Waveforms

LM1871 TX			LM1872 RX		
PIN CONDITIONS		TRANSMITTED WAVEFORM	BINARY PULSE COUNT	DIGITAL OUTPUTS	
PIN 5 (CH A)	PIN 6 (CH B)	t_F		CH A	CH B
OPEN	OPEN		100	OFF	OFF
GND	OPEN		101	ON	OFF
OPEN	GND		110	OFF	ON
GND	GND		111	ON	ON

FIGURE 3. Digital Channel Encoding and Decoding via Pulse Count Modulation

Circuit Description (Continued)

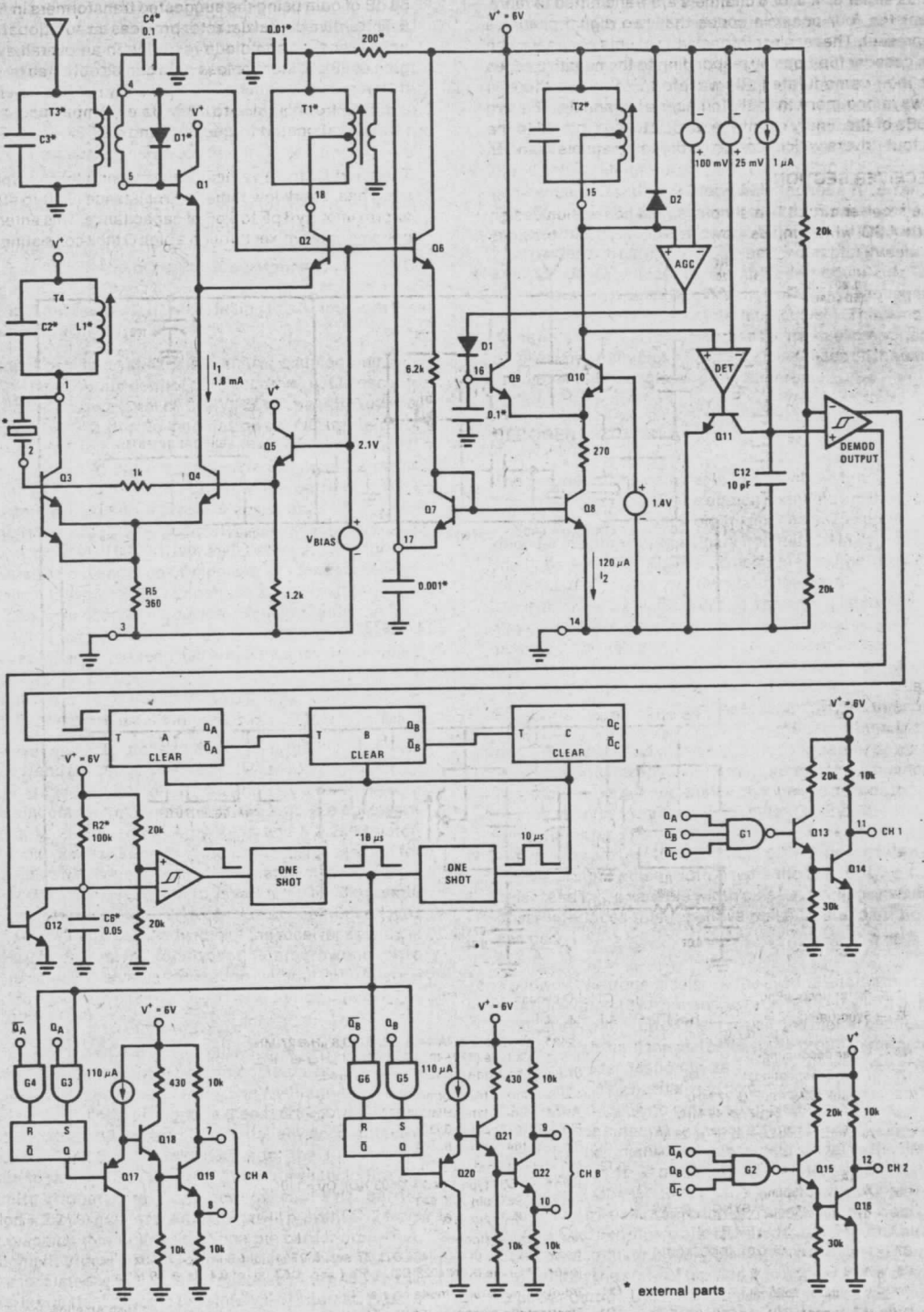
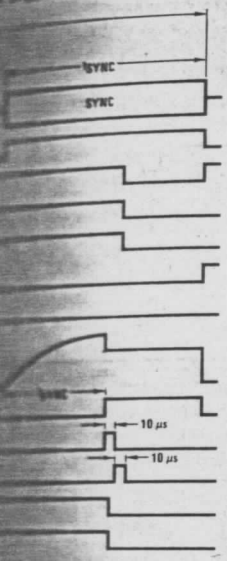


FIGURE 4. Simplified Schematic Diagram

...transmitter is equipped to transmit up to *six* ...with the companion LM1872 receiver uses to ...and 2 digital channels. The receiver ...demodulated RF waveform from the ...negative edge triggering a cascade of ...dividers called the A, B, and C toggle flip-... By "examining" all three flip-flop outputs ...up to 6 unique channel time intervals ...ed and recovered. Only the first two ...ually decoded however and outputted by ...the rest being used for identification of two ...channels. In passing digital information, ...modulation scheme is used whereby dif-...of channel pulses are transmitted by ...number of fixed width channels following the ...with analog channels 1 and 2 *(see Figure 3)*.



LM1872 RX		
BINARY PULSE COUNT	DIGITAL OUTPUTS	
	CH A	CH B
100	OFF	OFF
101	ON	OFF
110	OFF	ON
111	ON	ON

...Count Modulation

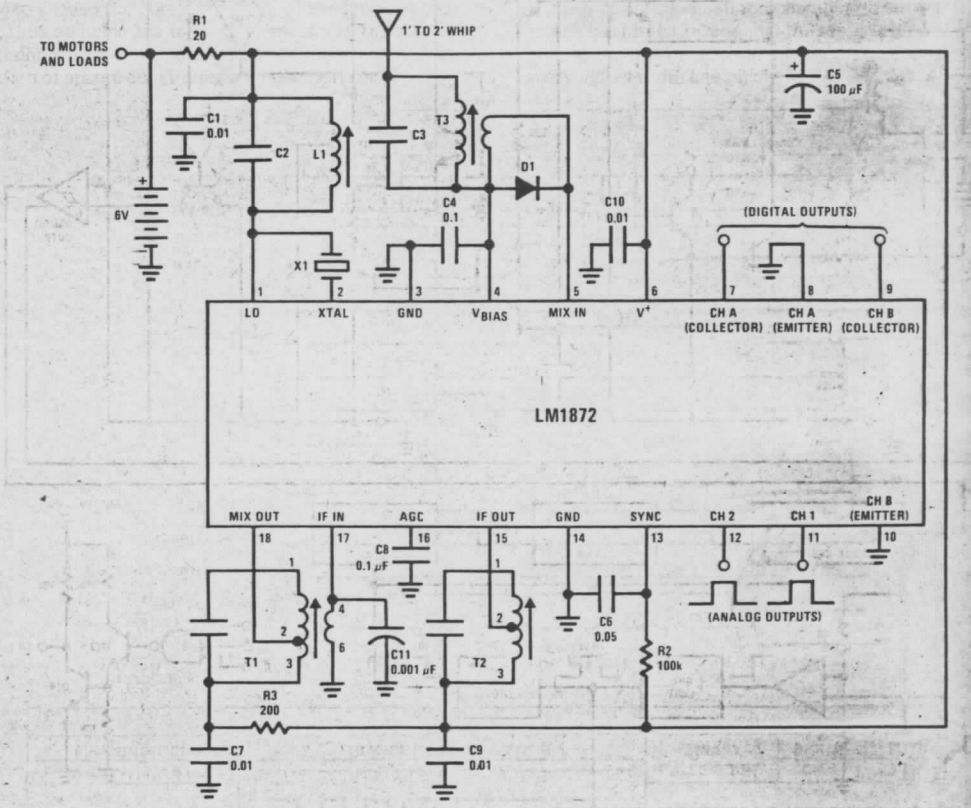
Circuit Description (Continued)

Thus either 3, 4, 5, or 6 channels are transmitted to represent the four possible codes that two digital channels represent. The receiver intrinsically counts channels with its decoder flip-flops by responding to the negative edges of the demodulated RF waveform of which there is always one more than the number of channels. The two LSBs of the binary count are read, latched, and fed to the output drivers which comprise digital channels A and B.

RECEIVER SECTION

The receiver circuit is a simple, single conversion design with AGC which mixes down to 455 kHz and provides 58 dB of gain using the suggested transformers in Fig 5. The active digital detector provides an additional 3(gain over a silicon diode resulting in an overall sys gain of 88 dB. More or less gain can be obtained by u different transformers. The frequency range of opera extends from 50 kHz to 72 MHz encompassing a v range of allocated frequency bands.

The short (1' to 2') vertical whip antenna that is typic used has a very low radiation resistance (0.5Ω to 4Ω) approximately 3 pF to 5 pF of capacitance. This anten coupled to the mixer through a high Q tank consisting c



R1 – Motor decoupling

R2 – Sync timer; $R2 = \frac{t_{SYNC}}{0.7\ C6}$, R2≤470k

R3 – Mixer decoupling

C1 – LO bypass; optional

C2 – LO tank; C2 = 43 pF @ 27 MHz
= 24 pF @ 49 MHz

C3 – Ant. input tank; C3 = 39 pF @ 27 MHz
= 24 pF @ 49 MHz

C4 – V_{BIAS} bypass

C5 – Motor decoupling

C6 – Sync timer; $C6 = \frac{t_{SYNC}}{0.7\ R2}$, C6 ≤0.5 µF

C7 – Mixer decouple; 0.01 µF≤C7≤0.1µF

C8 – AGC

C9 – IF bypass; optional

C10 – V^+ bypass; 0.01 µF≤C10≤0.1µF

C11–LO bypass

L1 –LO coil
Toko* 10k type (KXNA-4434 DZ) 9T; 0.8 µH@27 MHz
Toko* 10k type (KEN-4028 DZ) 6T; 0.4 µH@49 MHz
L1 could be made a fixed coil, if desired.

T1 –455 kHz mixer transformer
Toko* 10 EZC type (RMC-202313 NO), Qu = 110
Pin 1–2, 131T; pin 2–3, 33T
Pin 1–3, 164T; pin 4–6, 5T

T2 –455 kHz IF transformer
Toko* 10 EZC type (RMC-402503 NO), Qu = 110
Pin 1–2, 98T; pin 2–3, 66T
Pin 1–3, 164T; pin 4–6, 8T

T3 –Ant. input transformer
Toko* 10k type (KXNA-4434 DZ), 3T sec. & 9T pri. of 0.8 µH @ 27 MHz
Toko* 10k type (KEN-4028 DZ), 1 1/2 T sec. & 6T pri. of 0.4 µH @ 49 MHz

X1 –3rd overtone parallel-mode crystal

D1 –Electrostatic discharge (ESD) protection

* Toko America, Inc.
5520 West Touhy Ave
Skokie, Ill. 60077
(312)677-3640 Tlx: 72

FIGURE 5. Typical Application Circuit for 27 MHz or 49 MHz

Circuit Description (Continued)

and T3. This tank effectively keeps strong out-of-band signals such as FM and TV broadcast from cross-modulating with the desired signal. When operating at 49 MHz or 72 MHz, CB interference is also effectively minimized. Image rejection is relatively low, however, being only 7 dB @ 49 MHz, but this does not present a problem due to the usual absence of strong interfering signals 910 kHz below the desired signal.

The antenna signal is stepped down and DC coupled to the mixer which consists of the emitter-coupled pair Q1 and Q2. Emitter-follower, Q1, feeds the common-base device, Q2, while effectively buffering the antenna from the LO energy delivered by Q4. Mixer transconductance is 4 mmhos at low frequency (1 MHz) falling to 3.3 mmhos at the upper end (72 MHz).

The local oscillator utilizes an emitter coupled pair, Q3 and Q4, for accurate control of mixer drive, I_1. Quiescently, Q3 and Q4 share I_1 set by 0.69V/R5, but healthy voltage swings at pin 2 due to oscillation of Q3 implement thorough switching of the differential pair. As a result, the full 1.8 mA of drive "tailgates" (switches) the mixer emitter coupled pair, Q1 and Q2. This current is well regulated from supply voltage changes by the V_{BIAS} circuitry. The TC of V_{BIAS} is positive by design in order to impress a positive TC on I_1 so as to compensate for the temperature dependence of bipolar transconductance in the mixer. Inasmuch as Q4 operates as an emitter-gated, common-base-connected device, excellent isolation between local oscillator and mixer is obtained. As long as pin 4 is properly bypassed, Q5 presents a low impedance to the base of Q4, resulting in low oscillator noise. The oscillator easily operates up to 72 MHz with overtone crystals operating parallel mode.

The mixer signal is stepped down from the high Q mixer tank, T1, and DC coupled to the IF via a secondary winding. The IF stage consists of Q7, Q8 and Q10 and delivers a transconductance of 4 mmhos @ 455 kHz. The quiescent current, I_2, is set at 120 μA by V_{BIAS} and a 6.2k resistor. Again, the positive TC of V_{BIAS} is used to compensate for the temperature dependence of transconductance. The impedance at the IF output, pin 15, is very high (≥800k) permitting the IF transformer, T2, to operate at near unloaded Q (110). The overall 3 dB bandwidth of the receiver section is 3.2 kHz (see characteristic curves); this is narrow enough to permit adjacent channel operation without interference yet wide enough to pass the 500 μs modulation pulses (t_M in *Figure 2*).

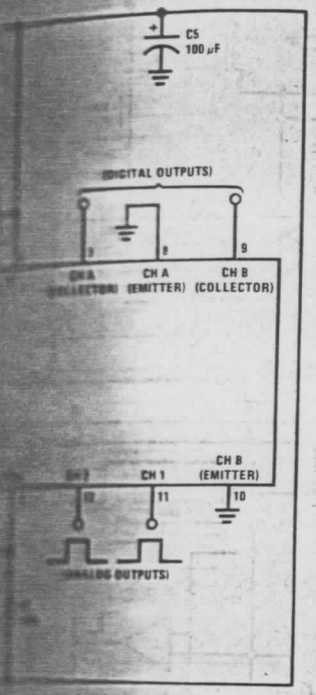
The IF signal is DC coupled to the digital detector which consists of a high gain precision comparator, a 30 μs integrator, and a supply-referred 25 mV voltage reference. Whenever the peak IF signal exceeds 25 mV, the comparator drives Q11 to reset the digital envelope detector capacitor, C12. Since it takes 30 μs for the 1 μA current source to ramp C12 to the 3V ($V^+/2$) necessary to fire the Schmitt trigger, the presence of 455 kHz carrier (period = 2.2 μs) greater than 25 mVp will prevent C12 from ever reaching this threshold. When the carrier drops out, the Schmitt trigger will respond 30 μs later. This delay (like that associated with the burst response of the 455 kHz IF tanks) is constant over the time interval of interest. Thus, it is of no consequence to timing accuracy because the LM1872 responds only to negative edges in the decoder.

AGC is provided only to the IF; the mixer having sufficient overload recovery for the magnitude of signals available from a properly operating (i.e. good carrier ON/OFF ratio) 10,000 μV/m transmitter. The AGC differential amplifier regulates the peak carrier level to 100 mV by comparing it to an internal 100 mV supply-referred voltage reference. The resultant error signal is amplified and drives Q9 via rectifier diode, D1, to shunt current away from Q10. C8 provides compensation for the AGC loop which spans a 70 dB range. The 100 mV AGC reference is accurately ratioed to the 25 mV detector reference to permit a controlled amount of brief carrier loss before dropping below detector threshold. Once into AGC, typically 60% amplitude modulation of the PWM carrier is possible before the detector will recognize the interference (see characteristic curves). This kind of noise immunity is invaluable when the troublesome effects of other physically close toys or walkie-talkies on the same or adjacent frequencies are encountered.

DECODER SECTION

The purpose of the decoder is to extract the time information from the carrier for the analog channels and the pulse count information for the digital channels. The core of the decoder is a three-stage binary counter chain comprising flip-flops A, B, and C. The demodulated output from the detector Schmitt-trigger drives both the counter chain and the sync timer (Q12, R2, C6, and another Schmitt trigger). When the RF carrier drops out for the first modulation pulse, t_M, the falling edge advances the counter (see *Figure 2*.) During the t_M interval the sync timer capacitor is held low by Q12. When the carrier comes up again for the variable channel interval, t_{CH}, C6 begins to ramp towards threshold ($V^+/2$) but is unable to reach it in the short time that is available. At the end of the t_{CH} period the carrier drops out again, the counter advances one more, and the sequence is repeated for the second analog channel. To decode the two analog channels, 3-input NAND gates G1 and G2 examine the counter chain binary output so as to identify the time slots that represent those channels. Decoded in this manner, the output pulse width equals the sum of t_M, a fixed pulse, and t_{CH}, a variable width pulse. A Darlington output driver interfaces this repetitive pulse to standard hobby servos.

Following the transmission of the second analog channel, a variable quantity from one to four, of fixed width pulses (500 μs) are transmitted that contain the digital channel information. Up until the end of the pulse group frame period, t_F, the decoder responds as if these fixed pulses were analog channels but delivers no outputs. At the conclusion of the frame the sync pulse, t_{SYNC}, is sent. Since t_{SYNC} is always made longer than the sync timer period ($t'_{SYNC} = 3.5$ ms), the sync timer will output a sync signal to the first of two cascaded 10 μs one-shots. The first one-shot enables AND gates G3→G6 to read the A and B flip-flops of the counter into a pair of RS latches. The state of flip-flop A, for example, is then stored and buffered to drive 100 mA sink or source at the channel A digital output. An identical parallel path allows the state of flip-flop B to appear at the channel B power output. Upon conclusion of the 10 μs read pulse, another 10 μs one-shot is triggered that resets the counter to be ready for the next frame.



the suggested transformers in *Figure* digital detector provides an additional 30 dB diode resulting in an overall system More or less gain can be obtained by using mers. The frequency range of operation kHz to 72 MHz encompassing a wide ed frequency bands.

vertical whip antenna that is typically low radiation resistance (0.5Ω to 4Ω) and pF to 5 pF of capacitance. This antenna is through a high Q tank consisting of C3

@ 27 MHz
@ 49 MHz

* Toko America, Inc.
5520 West Touhy Ave.
Skokie, Ill. 60077
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Application Hints

A typical application circuit for either 27 MHz or 49 MHz is shown in *Figure 5*. Using the recommended antenna input networks and driving the circuit through the antenna simulation network of *Figure 6*, a solid decoded output occurs for 10 μV and 12 μV input signals at 27 MHz and 49 MHz respectively.

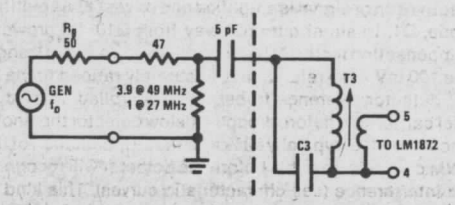


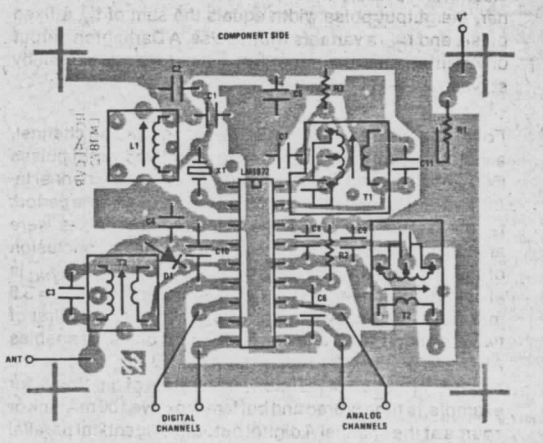
FIGURE 6. Antenna Simulation Network

This sensitivity has been determined empirically to be optimum for toy vehicle applications. Less gain will reduce range unacceptably and more gain will increase susceptibility to noise. However, should the application require greater range (>50m for a land vehicle, for example), either the antenna could be lengthened beyond 2′ and/or receiver sensitivity could be improved. There are a number of ways to alter the sensitivity of the receiver. Decreasing the turns ratio of input transformer, T3, for example, will couple more signal into the mixer at the expense of lower tank Q due to mixer loading. Moving the primary tap on mixer transformer, T1, further from the supply side and/or decreasing the primary to secondary turns ratio will also increase gain. For example, just changing T1 from a 32:1 primary to secondary ratio to a 5:1 turns ratio (Toko #RMC202202) will double 49 MHz sensitivity (6 μV vs 12 μV). Mixer tank Q will be affected but overall 3 dB BW will remain largely unchanged. The primary tap on the IF transformer, T2, can also be adjusted (further from the supply side) for higher gain, but it is possible to cause the AGC loop to oscillate with this method.

Narrow overall bandwidth is important for good receiver operation. The 3.2 kHz 3 dB bandwidth of the circuit in *Figure 5* is just wide enough to pass 500 μs carrier dropout pulses, t_M, yet narrow enough to hold down electrical noise and reject potentially interfering adjacent channels. In the 49 MHz band, the five frequencies available are only 15 kHz apart. Should only two frequencies be used simultaneously, these channels could be chosen 60 kHz apart. Should three frequencies be used, the spacing could be no more than 30 kHz. At four or five frequencies, 15 kHz spacings must be dealt with, making narrow bandwidth highly desirable. Even at 27 MHz, where allocated frequencies are 50 kHz apart, the proliferation of CB stations only 10 kHz away represents a formidable source of interference. The response of the circuit of *Figure 5* is 34 dB and 56 dB down at 15 kHz and 50 kHz away, respectively (see characteristic curves).

The sync timer should have a timeout, t'_{SYNC}, set longer than the longest channel pulse transmitted, but shorter than the shortest sync pulse, t_{SYNC}, transmitted. Using the component values in *Figure 5*, $t'_{SYNC} = 3.5$ ms, which works well with a transmitted synce pulse, $t_{SYNC} \geq 5$ ms.

Numerous bypass capacitors appear in the circuit of *Figure 5*, not all of which may be necessary for good stability and performance. A low cost approach may eliminate one or more of the capacitors C1, C9, C10, and C11. The cleaner and tighter the PCB layout used, the more likely is the case that bypass capacitors can be eliminated. In the case of marginal board stability, increasing the size of capacitors C7, C9, and C10 to 0.1 μF may prove helpful. If the PCB layout and parts loading diagram shown in *Figure 7* is used, the circuit will be quite stable up to 72 MHz.



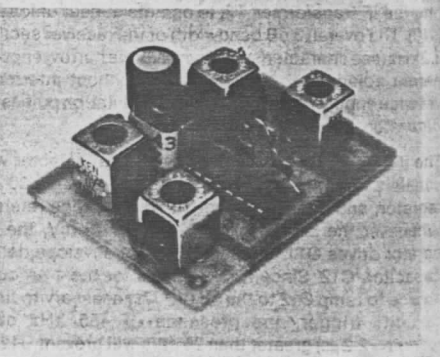


FIGURE 7. PCB Layout, Stuffing Diagram and Complete RX Module for Typical Application Circuit of *Figure 5*

Application Hints (Continued)

The digital channel output devices have significant drive capability; they can typically sink 100 mA and posses a 70 saturation resistance. Through their emitters they can source 100 mA up to 1V above ground for driving grounded NPNs and SCRs. Unfortunately, this kind of drive capability can cause thermally induced chip destruction unless total power dissipation is limited to less than 1000 mW. It is good practice and highly recommended to allow the digital output devices to fully saturate at all times (sinking or sourcing) and to limit the current at saturation to no more than 100 mA. For extra drive the two digital outputs can always be summed by connecting pin 7 to pin 9.

The IF frequency is not constrained to be 455 kHz. Operation is limited on the high end to about 1 MHz due to the frequency response limitations of the active detector. The low end is limited to about 50 kHz due to the envelope detector integration time *(Figure 4)*.

Receiver Alignment

The receiver alignment procedure is relatively straightforward because of an absence of interaction between the adjustments. First, the oscillator is tuned by adjusting L1 while monitoring the LO signal at pin 2 with a low capacity (≅10 pF) probe. During tuning the amplitude will rise, peak, and then abruptly quit. Adjust the coil away from the quitting point and just below the amplitude peak.

In order to properly tune T1, T2, and T3, the RF signal must be provided through the receiver antenna by the specific transmitter which is to be used with that specific receiver. This is because the crystals which are commonly used with these systems may have tolerances as loose as ±0.01%. At 49 MHz the resultant ±5 kHz deviation could easily put the incoming signal out of the 3.2 kHz receiver IF bandpass. The signal should be coupled through the receiving antenna to ensure proper loading of the T3 input tank.

Alignment is easier with a defeated AGC, which is accomplished by merely grounding pin 16. The amplitude of the 455 kHz signal at pin 15 is used to guide alignment. Care should be exercised that the signal swing not exceed roughly 400 mVp or diode, D2, in *Figure 4* will threshold and clamp the waveform. Also note that a standard 10 pF probe at pin 15 will shift the IF tank frequency an undesirable 2 kHz. Unless a lower capacity probe is available, it is recommended that the signal be monitored at the unused secondary of T2. Although the signal amplitude would be down by a factor of 8.25 relative to pin 15, up to 50 pF probe capacitance could be tolerated with negligible frequency shift.

The incoming signal is obtained by removing the antenna from the transmitter and then locating the transmitter at a sufficient distance from the receiver to give a convenient signal level (≤400 mVp) at pin 15. T3, T1, and T2 are then tuned for maximum signal.

Applications

Operation at 72 MHz

The licensed 72 MHz band is popular among hobby enthusiasts for controlling aircraft. The higher transmitted power levels that the FCC allows yield much greater operating range and the frequency band is uncluttered relative to 27 MHz. Elevated frequencies such as 72 MHz are no problem with the LM1872. The part is stable and will provide good sensitivity and selectivity at that frequency. The application circuit in *Figure 8* will provide a set of solid decoded outputs for <2 μV of signal at the antenna input, which is designed to match the 100Ω resistive impedance of the 1/4 wavelength antenna. IF bandwidth is a respectable 3.2 kHz. For good immunity to overload from a very closely (antennas touching) operating high power transmitter, the transmitter design should emphasize a high carrier ON/OFF ratio. Using the LM1871 as a low power exciter to drive one or more external class C power amplifier stages will result in a simple, acceptable, low cost transmitter at 72 MHz.

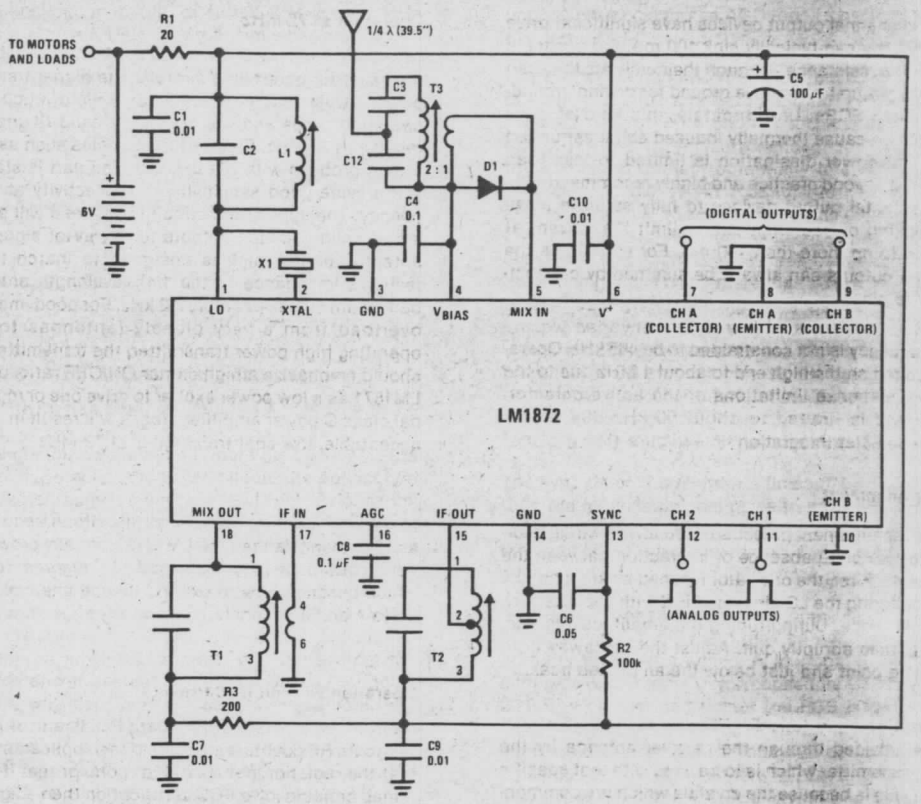
Inasmuch as many hobby applications require more analog channels than the LM1872 normally provides, particular attention should be paid to *Figures 10 and 12* which describe how to expand analog channel capacity up to 4 and 6 channels, respectively.

Operation with an IR Carrier

An infra-red (or visible) light data link is a useful alternative to its RF counterpart. Should the application demand that the radiation not leave the room, or that it be directional, or not involve FCC certification then a light carrier should be given consideration. The principal drawbacks to this approach include short range (≤20 ft.) and high transmitter power consumption. There is little that can be done to dramatically improve range, but short burst-type operation of the transmitter will still permit battery operation.

The information link *(Figure 9a)* consists of a light carrier amplitude modulated by a 455 kHz subcarrier. The subcarrier in turn is modulated by the normal Pulse Width/Pulse Count Scheme produced be the LM1871 encoder. A husky, focused LED is used as the transmitter running Class A 100% modulated with an average current drain of 50 mA to 500 mA depending upon range requirements. The detector consists of a large area silicon PN or PIN photodiode for good sensitivity. The LM1872 will directly interface to such a diode and give very good performance. Only a few nanoamps of photo current from D1 are required to threshold the detector. Ambient light rejection is excellent due to the very narrow bandwidth (≅3 kHz) that results from the use of three high Q 455 kHz transformers, T1, T2, and T3. Note that the LO has been defeated and the mixer runs as a conventional 455 kHz amplifier. Otherwise, circuit operation is the same as if an RF carrier were being received.

Applications (Continued)



R1 – Motor decoupling

R2 – Sync timer; $R2 = \frac{t_{SYNC}}{0.7\ C6}$, $R2 \leq 470k$

R3 – Mixer decoupling

C1 – LO bypass; optional

C2 – LO tank; C2 = 22 pF @ 72 MHz

C3 – Ant. input tank; C3 = 24 pF @ 72 MHz

C4 – V_{BIAS} bypass

C5 – Motor decoupling

C6 – Sync timer; $C6 = \frac{t_{SYNC}}{0.7\ R2}$, $C6 \leq 0.5\ \mu F$

C7 – Mixer decouple; $0.01\ \mu F \leq C7 \leq 0.1 \mu F$

C8 – AGC

C9 – IF bypass; optional

C10 – V^+ bypass; $0.01\ \mu F \leq C10 \leq 0.1 \mu F$

C12 – Ant. input tank; C12 = 160 pF @ 72 MHz

L1 – LO coil
Toko* 10k type (KENC) 4T; 0.2 µH @ 72 MHz
L1 could be made a fixed coil, if desired.

T1 – 455 kHz mixer transformer
Toko* 10 EZC type (RMC-502182), Qu = 110
Pin 1-2, 82T; pin 2-3, 82T
Pin 1-3, 164T; pin 4-6, 30T

T2 – 455 kHz IF transformer
Toko* 10 EZC type (RMC-502503), Qu = 110
Pin 1-2, 82T; pin 2-3, 82T
Pin 1-3, 164T; pin 4-6, 8T

T3 – Ant. input transformer
Toko 10k type (KENC), 4T sec. & 2T pri. of 0.2 µH @ 72 MHz

X1 – 5th overtone crystal, parallel-mode, 72 MHz

D1 – Electrostatic discharge (ESD) protection

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FIGURE 8. 72 MHz Receiver Circuit

In a practical remote data link, the transmitter could be battery operated and set up to transmit for brief intervals only in order to save power. The brief transmission could be used to set or reset the digital output latches in the LM1872 and /or command new motor positions via the analog channels. After transmission, the commands would be stored electrically in the case of the digital channels and the mechanically in the case of the analo channels.

As a final note, if the case of D1 is connected to th anode rather than the cathode, the circuit of *Figure 9* should be used at the input to maintain electromagneti shielding.

Applications (Continued)

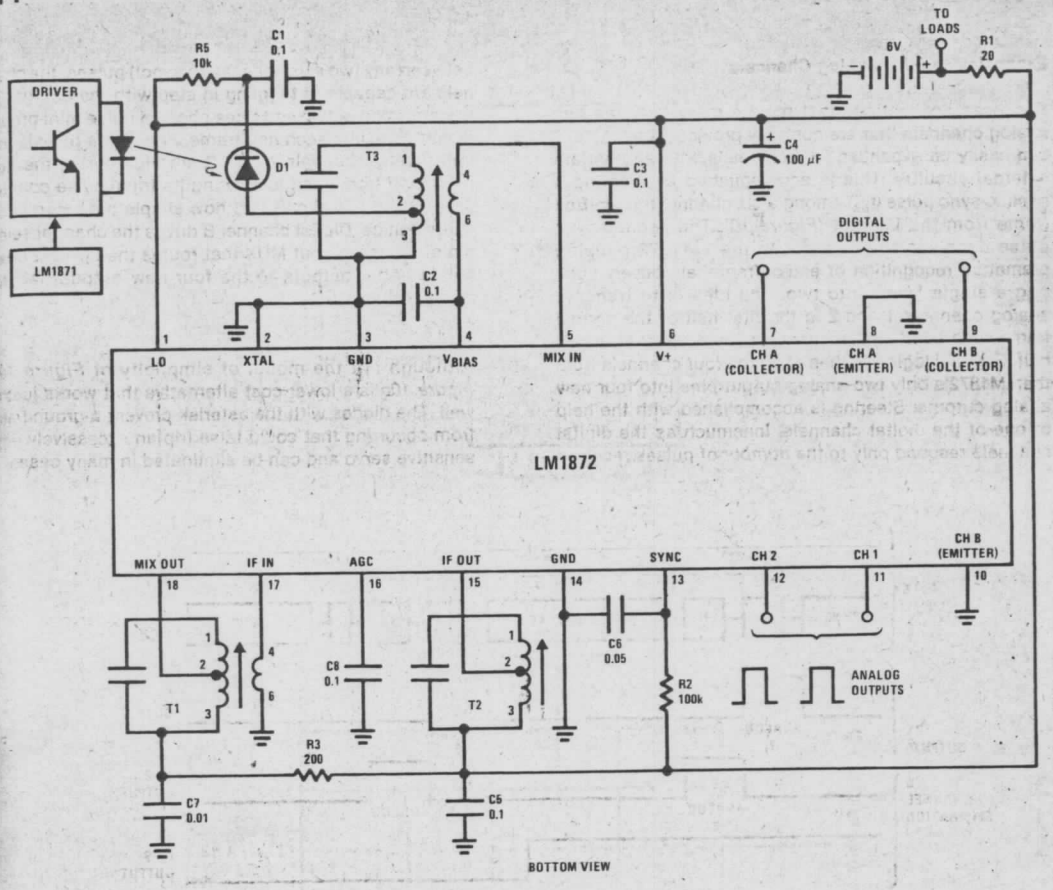

FIGURE 9a. IR Type Data Link

R1 – Load decoupling

R2 – Sync timer; $R2 = \frac{t}{0.7\ C6}$, $R2 \leq 470k$

R3 – Preamp decoupling

R5 – Photodiode decoupling

C1 – Photodiode decoupling

C2 – V_{BIAS} bypass

C3 – V^+ bypass

C4 – Load decoupling

C5 – IF bypass; optional

C6 – Sync timer; $C6 = \frac{t_{SYNC}}{0.7\ R2}$, $C6 \leq 0.5\ \mu F$

C7 – Preamp decoupling

C8 – AGC

T1 – 455 kHz preamp transformer
Toko* 10 EZC type (RMC-502182), Qu = 110
Pin 1-2, 82T; pin 2-3, 82T
Pin 1-3, 164T; pin 4-6, 30T

T2 – 455 kHz IF transformer
Toko* 10 EZC type (RMC-402503), Qu = 110
Pin 1-2, 98T; pin 2-3, 66T
Pin 1-3, 164T; pin 4-6, 8T

T3 – 455 kHz input transformer
Toko* 10 EZC type (RMC-202313), Qu = 110
Pin 1-2, 131T; pin 2-3, 33T
Pin 1-3, 164T; pin 4-6, 5T

D1 – PN or PIN Silicon Photodiode

Photodiode, D1		Active Area (cm^2)
Vactec	VTS 5088	0.18
Vactec	VTS 6089	0.52
UDT	PIN 6D or 6 DP	0.20
UDT	PIN 220 DP	2.0
Siemens	BPY 12	0.20

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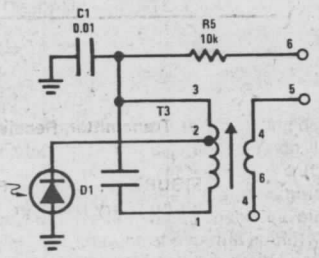


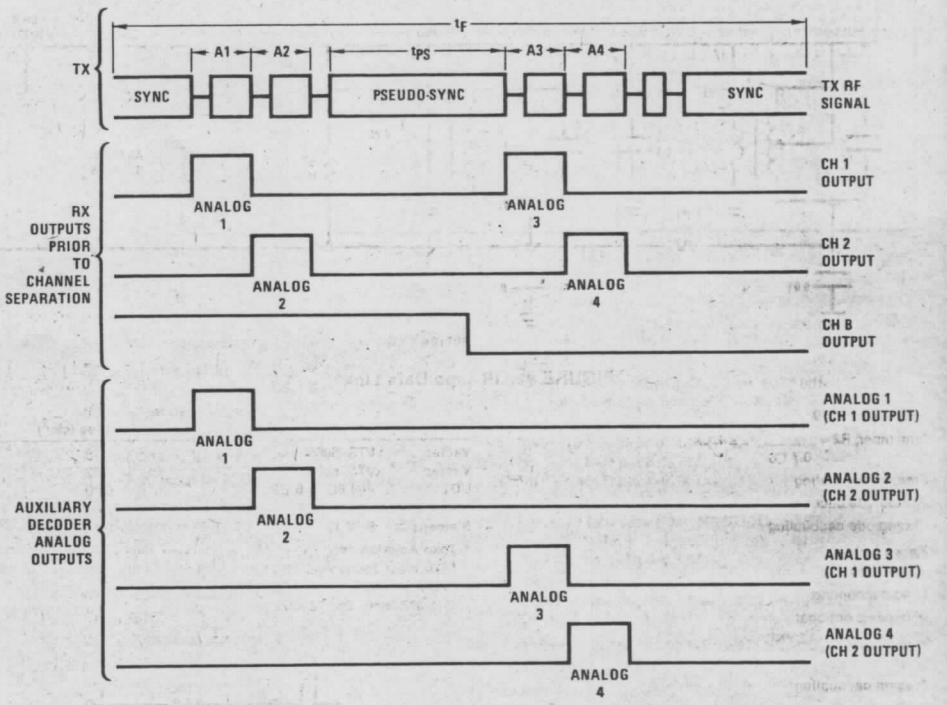
FIGURE 9b. Input Stage Where the Case of D1 is Connected to the Anode

Applications (Continued)

Expansion to Four Analog Channels

For those applications that require more than the two analog channels that are normally provided, the LM1872 can easily be expanded to 4 channels with appropriate external circuitry. This is accomplished by creating a pseudo-sync pulse (t_{PS}) among a six channel transmitted frame from the LM1871 *(Figure 10)*. The pseudo-sync pulse deceives the decoder in the LM1872 causing premature recognition of end-of-frame, effectively splitting a single frame into two. The idea is to transmit analog channels 1 and 2 in the first half of the normal frame period and analog channels 3 and 4 in the second half. External logic will then steer the four channels from the LM1872's only two analog output pins into four new analog outputs. Steering is accomplished with the help of one of the digital channels. Inasmuch as the digital channels respond only to the *number* of pulses received between any two sync (or pseudo-sync!) pulses, the channels are capable of toggling in step with the alternating transmission of two and three channel pulse mini-groups occurring within each half frame. *Figure 10a* reveals that both digital channels A and B are high during the dual pulse half frame and low during its triple pulse counterpart. *Figure 10b* shows just how simple the external circuitry can be. Digital channel B drives the channel select pin of a quad 2-input MUX that routes the LM1872 channels 1 and 2 outputs to the four new outputs labeled analog 1 through 4.

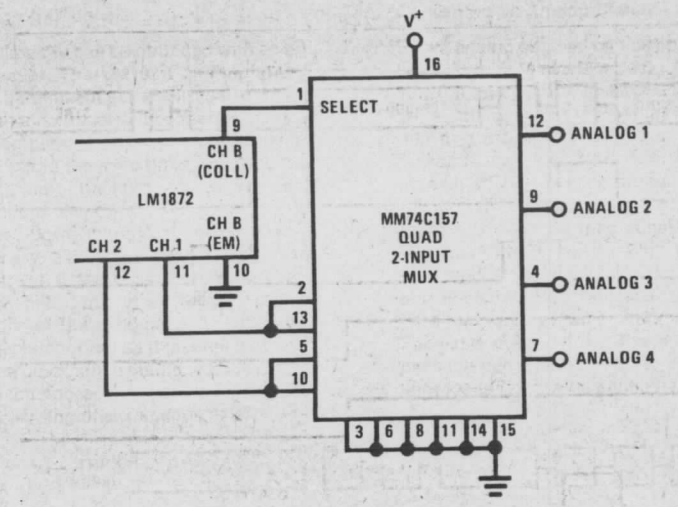
Although not the model of simplicity of *Figure 10b*, *Figure 10c* is a lower cost alternative that works just as well. The diodes with the asterisk prevent a ground step from occurring that could false trip an excessively edge sensitive servo and can be eliminated in many cases.



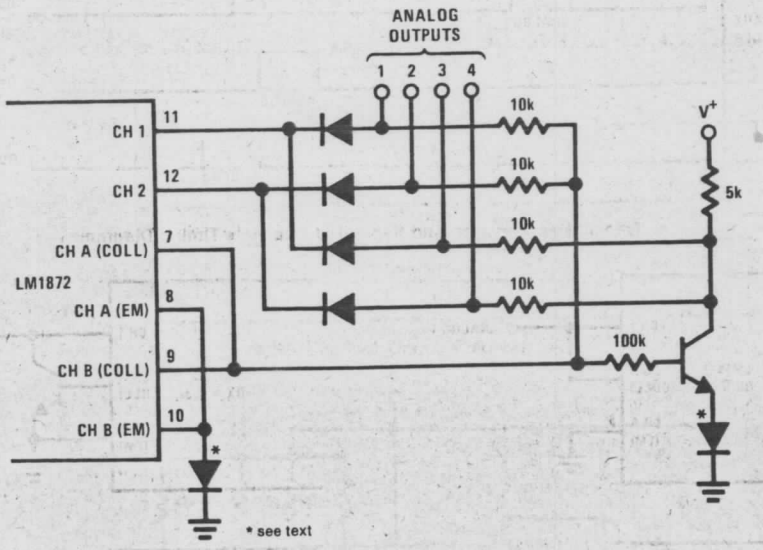
a) Transmitter, Receiver, and Auxiliary Decoder Timing Diagram

FIGURE 10. Deriving Four Analog Channels Through the Use of an Auxiliary Decoder

Applications (Continued)



b) Simple Decoding of Four Analog Channels with CMOS



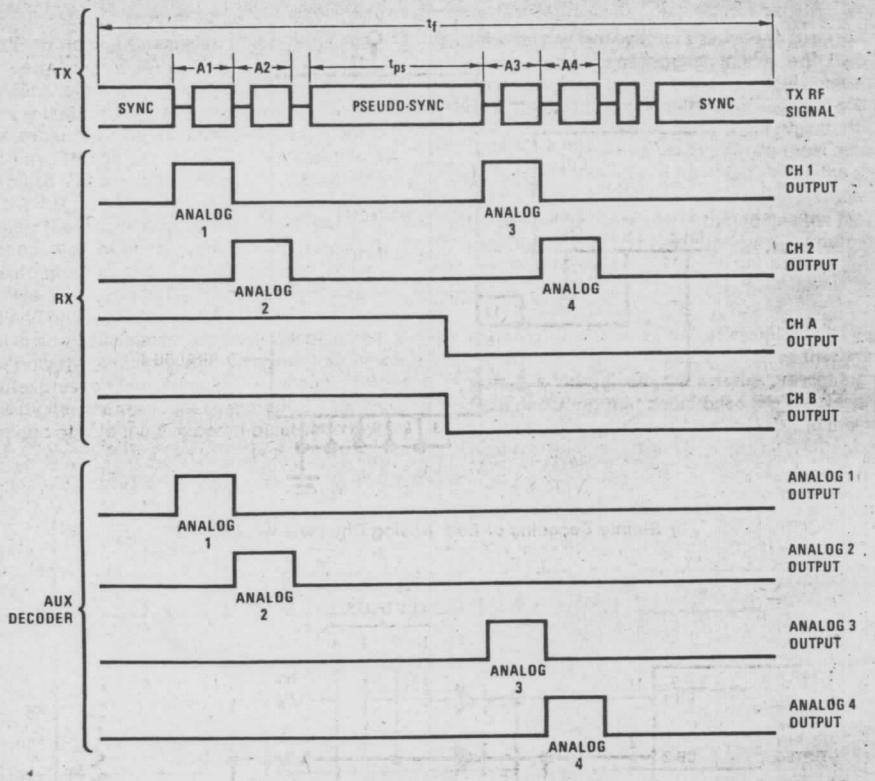
c) Low-Cost Decoding of Four Analog Channels with DTL

FIGURE 10. Deriving Four Analog Channels Through the Use of an Auxiliary Decoder

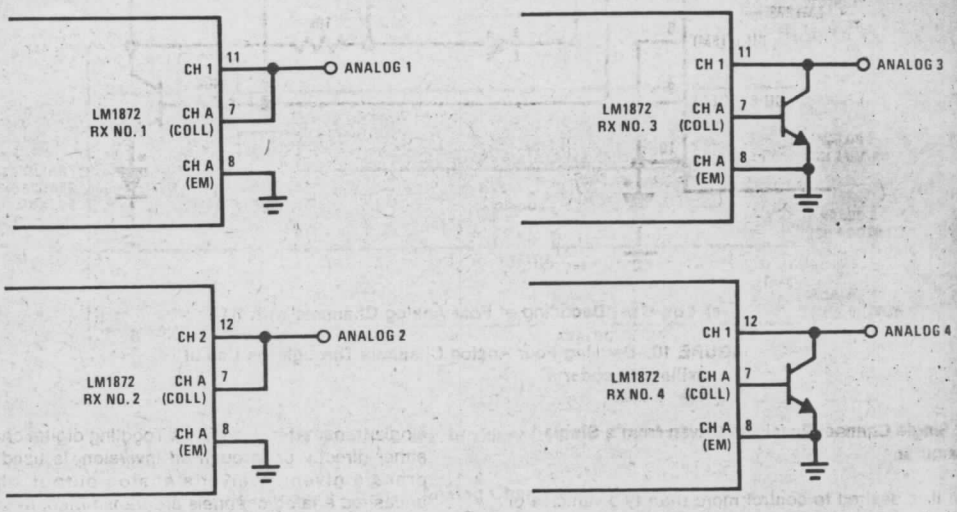
Four Single Channel Receivers Driven from a Single Transmitter

When it is desired to control more than two vehicles or remote stations with the analog information from a single transmitter, the LM1872 can be put to the task. By utilizing the frame splitting technique previously described in *Figure 10*, up to four independent single analog channel receivers can be made to operate from a single transmitter *(Figure 11)*. Toggling digital channel A, either directly or through an inversion, is used to suppress a given receiver's analog output when the undesired analog channels are transmitted. In this manner, only the desired analog channel is outputted at each receiver. The amount of external circuitry required to do this is minimal; two receivers require a single transistor apiece while the other two receivers need no extra parts at all.

Applications (Continued)



a) Transmitter, Receiver, and Separated Channels Timing Diagram



b) Simple Channel Separation with Two External Transistors

FIGURE 11. Obtaining Four Independent Single Analog Channel Receivers from a Single Common Transmitter

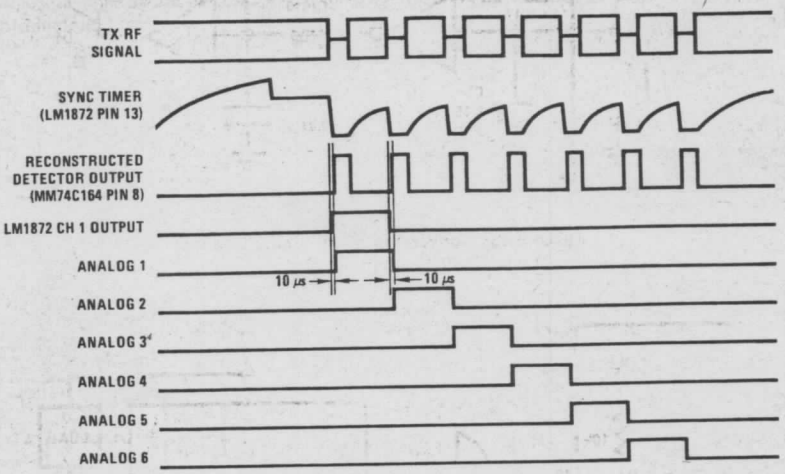
Applications (Continued)

Expansion to Six Analog Channels

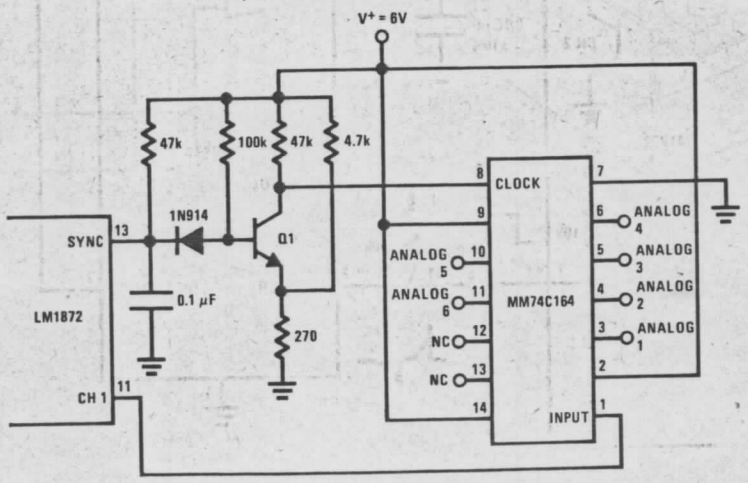
Still greater analog capacity can be obtained with an outboard auxiliary decoder. The LM1872, a simple comparator, and an 8-bit parallel-out serial shift register comprise a six analog channel receiver/decoder *(Figure 12)*. The one transistor comparator reconstructs the detector output of the LM1872 from the sync timer waveform and feeds it to the clock input of the shift register. The channel 1 output then loads a "one" into the register and the clock shifts the "one" down the line of analog channel outputs in accordance with the time information from the detector output. Note that the reconstructed detector waveform lags the channel 1 output very slightly (≅10 μs) due to the finite slope of the sync capacitor discharge edge. This delay is very important as it insures that channel 1 is high when the clock strikes initially (thus loading a "1") and low for each subsequent positive clock edge (thus preventing the loading of extraneous "1's").

Converting an Analog Channel to a Digital Channel

Either analog channel can be converted to a digital channel with the aid of a low cost CMOS hex inverter *(Figure 13)*. The internal 10k resistor and external capacitor, C1, set a time constant (1 ms) that falls between a short (0.5 ms) and a long (2 ms) transmitted pulse option. For pulses longer than 1 ms, the first inverter will pull low momentarily once each frame. Repetitive discharges of C2 prevent it from ever reaching threshold ($V^+/2$) because the R1 C2 time constant is set longer (70 ms) than the frame period. With the inverter input below threshold, Q1 will energize the load. For analog output pulses shorter than 1 ms, the first inverter will back bias D1 allowing C2 to ramp past threshold and Q1 to go off. *For extra output drive, the remaining inverters in the package can be paralleled to drive Q1. Alternatively, for light loads Q1 can be eliminated altogether.



a) Six Channel Timing Diagram



b) Six Channel Auxiliary Decoder

FIGURE 12. Deriving Six Analog Channels

Applications (Continued)

Where only one of the two available analog channels needs conversion to a digital format, the LM555 approach offers simplicity combined with up to 150 mA of output drive *(Figure 14)*. The trailing edge of CH 1's output pulse is used to reset the timer in preparation for comparing CH 2's pulse width to the time constant (1.1 ms) set by the internal 10k resistor and C1. For CH 2 pulse widths greater than 1.1 ms C1 ramps to threshold, setting an internal latch in the LM555 and causing t load to be energized. Due to the timing of the reset puls however, the LM555 output will go high again for 1.1 m during the next pulse comparison cycle thus producin an ON state duty cycle of about 95%. For most commo ly encountered loads such as motors, solenoids, lamp and horns, this is of little consequence. The OFF sta duty cycle is 100%.

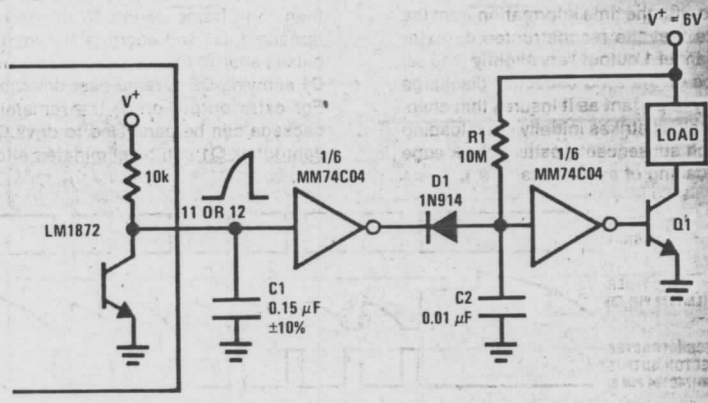


FIGURE 13. Conversion of an Analog Channel to a Digital (On/Off) Channel

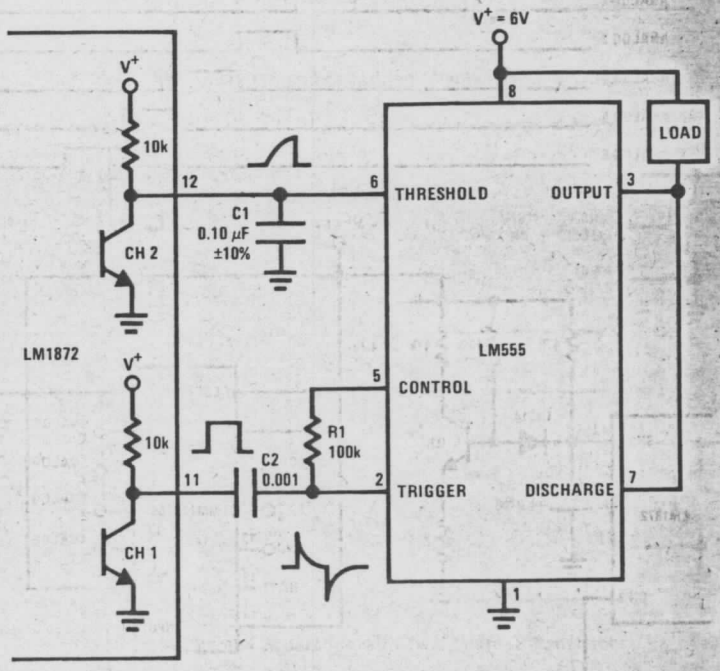


FIGURE 14. Simple Conversion of an Analog to a Digital Channel

Applications (Continued)

Bridge Driving a Motor

The two digital channels can be used to propel a car forward, off, and reverse without the need for a costly servo *(Figure 16)*. The 100 mA digital output capability is used to drive a bridge of four transistors with Q5 added as a protection device. Should an erroneous command to power both sides of the bridge occur (as may happen due to noise with the car out of range) the large motor drive transistors would fight one another resulting in the thermal destruction of one or more of those devices. But Q5 will disable the left side of the bridge whenever the right side is powered preventing the problem from ever occurring. The motor noise suppression network shown has proven to be especially effective in reducing electrical noise and is therefore highly recommended.

Noise Integration of a Digital Channel

Commonly available inexpensive DC motors are a formidable source of electromagnetic interference. Radiation can come from the power feed leads and/or directly from the brushes. Usually proper lead dress and board orientation coupled with a good filter network (see *Figure 16*) will eliminate any problems. In particularly stubborn cases of motor interference, the digital channels may experience more objectionable interference than the analog channels. This is generally not because the digital channels are more susceptible, but rather because the type of load they typically drive (i.e. a horn) will make more of a nuisance of itself than a typical analog load (i.e. a steering servo) when subjected to interference.

Straightforward time integration of the digital channel outputs works very well with any type or degree of motor interference. The simple circuits of *Figure 17* integrate over a period of about three frames (70 ms) and have approximately equal delay either going off or coming on.

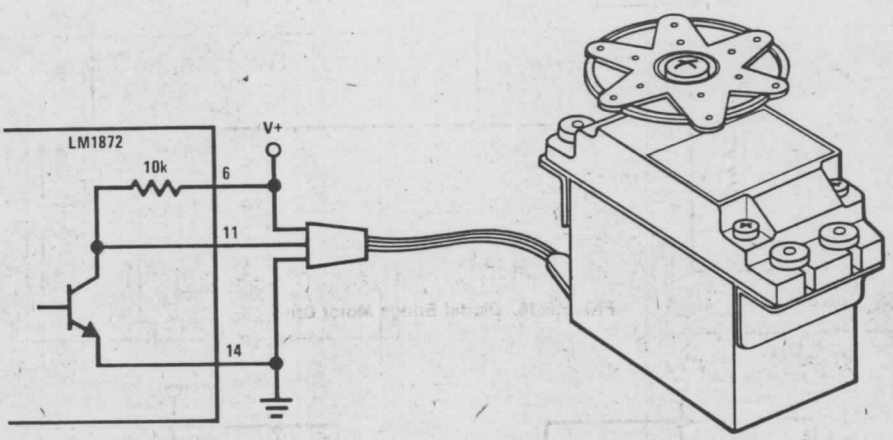


FIGURE 15. Interfacing Directly to Standard Hobby Servos

Applications (Continued)

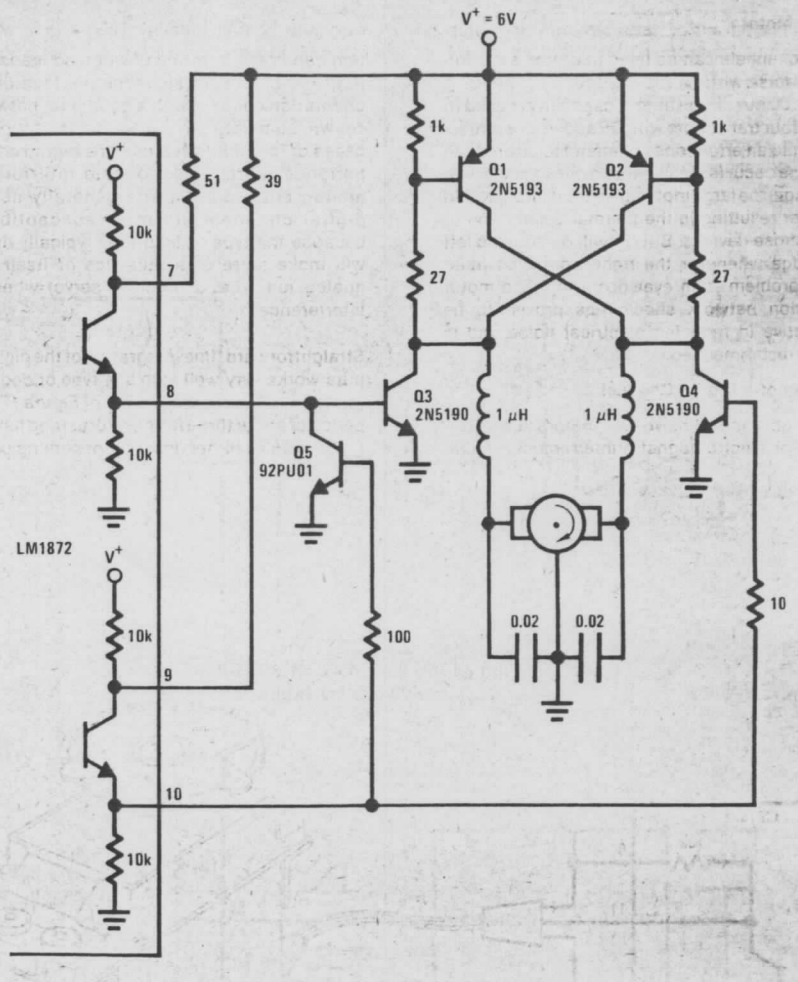
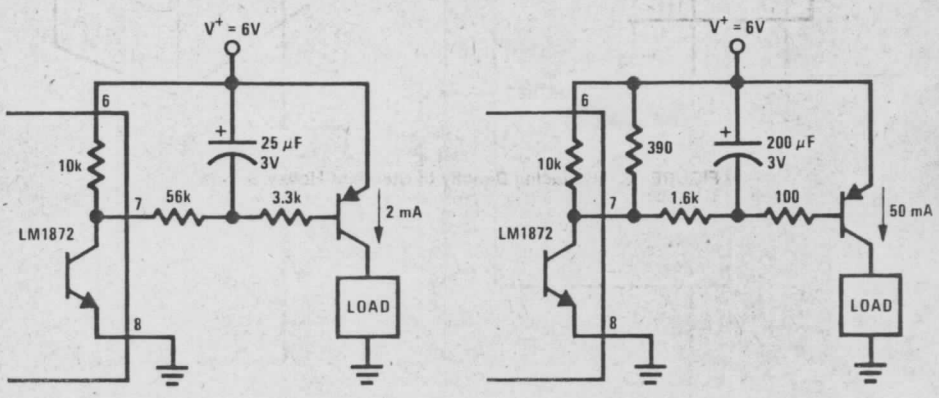


FIGURE 16. Digital Bridge Motor Drive



a) Low Current Load

b) High Current Load

FIGURE 17. Integrating a Digital Channel Output to Achieve Noise Immunity